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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,153	08/06/2001	Dov Moran	M01/20	3977

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EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/922,153	MORAN, DOV	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19, 22-27 and 36-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,22-27,36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed December 21, 2006 in response to PTO Office Action mailed September 21, 2006. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 22, 23 and 25 have been amended. Claim 28 has been canceled. No claims have been added. As a result, claims 19, 22-27 and 36-37 are now pending in this application.

3. The objections to claims and the rejections of claims under double patenting as well as 35 U.S.C. 112, second paragraph has been withdrawn due to amendments filed December 21, 2006.

Response to Arguments

4. Applicant's arguments with respect to claims 19, 22-27 and 36-37 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 19, 22-27 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson et al (US 6,601,167).

As per claim 19, Gibson discloses a method for booting a system (abstract), the method comprising:

providing a flash based unit in the system for storing the boot code to be executed (UltraNAND 32, fig.1, col. 3, lines 30-31), said flash-based unit comprising a flash memory of a restricted type, being characterized in that code cannot be directly executed from said flash memory (col. 1, lines 37-42, individual addresses are not accessible);

sending a busy signal to said processor (col. 3, lines 45-48, upon initialization, boot loader inhibits the processor and thereby prevents it from attempting to execute instruction);

transferring said portion of the boot code (col. 4, lines19-21);

removing said busy signal (where it is understood that when memory device is in process of downloading data for execution, it is required to send "busy signal" to executing entity to hold off the execution and once the required data is transferred, the execution can resume by removing the busy signal, col. 10, lines 33-43).

However, Gibson fails to teach a volatile memory component and loading portion of boot code to volatile memory and processor reading portion of boot code from volatile memory as required by the claim. Gibson teaches use of on-chip boot loader implemented as a state machine instead of random access memory (volatile memory component) to perform the task of initializing flash-based unit (col. 3, lines 44-59) and loading first portion of boot code to output registers of flash to be executed by processor (col. 6, lines 61-67). It is readily apparent from Gibson that flash based unit with on-chip volatile memory component is known in the art (col. 5, line 65 – col. 6, line 12). Thus it would have been obvious to one having ordinary skill in the art at the time of the invention to use volatile memory in the system of Gibson to improve the system performance.

As per claim 22, Gibson discloses a method for booting a system (abstract), the method comprising:

providing a flash based unit in the system for storing the boot code to be executed (UltraNAND 32, figs.1 and 8, col. 3, lines 30-31), said flash-based unit comprising a flash memory of a restricted type, being characterized in that code cannot be directly executed from said flash memory (col. 1, lines 37-42, individual addresses are not accessible);

sending a busy signal to said processor (col. 3, lines 45-48, upon initialization, boot loader inhibits the processor and thereby prevents it from attempting to execute instruction);

transferring said portion of the boot code (col. 4, lines19-21);

removing said busy signal (where it is understood that when memory device is in process of downloading data for execution, it is required to send "busy signal" to executing entity to hold off the execution and once the required data is transferred, the execution can resume by removing the busy signal, col. 10, lines 33-43).

However, Gibson fails to teach a volatile memory component and loading portion of boot code to volatile memory and processor reading portion of boot code from volatile memory as required by the claim. Gibson teaches use of on-chip boot loader implemented as a state machine instead of random access memory (volatile memory component) to perform the task of initializing flash-based unit (col. 3, lines 44-59) and loading first portion of boot code to output registers of flash to be executed by processor (col. 6, lines 61-67). It is readily apparent from Gibson that flash based unit with on-chip volatile memory component is known in the art (col. 5, line 65 – col. 6, line 12). Thus it would have been obvious to one having ordinary skill in the art at the time of the invention to use volatile memory in the system of Gibson by loading first portion of boot code to volatile memory to improve the system performance.

Gibson further teaches that transferring first portion of boot code containing a command for copying a second portion of the system code (col. 2, lines 31-36, col. 5, lines 9-19);

executing said first portion of the boot code by said processor to boot the system (col. 4, lines 8-44).

As per claim 23, Gibson teaches transferring a second portion of boot code to volatile memory component (col. 2, lines 33-40).

Claims 24-27 are also rejected under same rationales as applied to claim 19 above.

Gibson further discloses a small portion of volatile memory to load initial portion of the boot code only sufficient for basic initialization of a system (col. 6, lines 7-8, col. 2, lines 28-31).

As per claim 36, Gibson discloses a flash-based unit separate from the processor (figs. 1 and 8).

As per claim 37, Gibson teaches sending busy signal to processor during power on signal (col. 3, lines 45-49).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach non-executable flash memory.

8. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

9. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

kmp

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
2-9-07

Kaushikkumar Patel
Examiner
Art Unit 2188